## *REMARKS*

In the foregoing amendments, claims 8, 15, and 21 are amended; and claim 24 is canceled without prejudice, disclaimer, or waiver. Claims 8-23 and 25-27 are now pending in the present application.

## I. Indication of Allowable Subject Matter

Applicants wish to express their appreciation for the Examiner's indication of allowable subject matter in which claims 12, 13, 19, 20, 26, and 27 would be allowable if re-written to include the subject matter of the base claim and any intervening claim. However, Applicants do not wish at this time to amend the claims in this manner.

## II. Response to 35 U.S.C. §102 Rejection

Claims 21-23 stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by *Keeth et al.* (U.S. Patent Application Publication No. 2002/0118563). Applicants respectfully traverse this rejection and contend that *Keeth et al.* fails to disclose each and every element of the claims, as amended.

Independent claim 21 is reproduced below:

21. A system comprising:

a register having a clock input and a data input;

a clock receiver for receiving a clock signal;

at least one clock buffer for driving the clock signal to the register;

a data receiver for receiving a data signal; and

at least one data delay device;

wherein the at least one data delay device is configured to substantially match the delay of the clock signal from the clock receiver to the clock input of the register with the delay of the data signal from the data receiver to the data input of the register; and

***wherein each of the at least one data delay device is a scaled down version of the at least one clock buffer with respect to size, power, and load.***

(Emphasis added)

*Keeth et al.* fails to disclose the above-highlighted features of claim 21. *Keeth et al.* does not teach a system having a register, a clock receiver, at least one clock buffer, a data receiver, and at least one data delay device, ***wherein each of the at least one data delay device is a scaled down version of the at least one clock buffer with respect to size, power, and load.*** Instead, *Keeth et al.* appears to disclose a clock terminal 11 connected to a latch 13 via conductive path 17 and a data terminal 15 connected to the latch 13 via conductive path 19. *Keeth et al.* further teaches that the conductive paths 17 and 19 are made to be approximately equal in length (see the Abstract and paragraphs 0017 and 0018), which provides certain advantages. However, making the length of conductive paths 17 and 19 is not the same as the claimed feature of a data delay device that is a scaled down version of a clock buffer with respect to size, power, and load.

For at least the reason that *Keeth et al.* fails to disclose this aspect of claim 21, it is believed that claim 21 is allowable over this reference. Also, claims 22 and 23 are believed to be allowable for at least the reason that they depend from allowable independent claim 21. Therefore, Applicants respectfully request that Examiner withdraw the rejection of these claims.

## III. Response to 35 U.S.C. §103 Rejections

Claims 8-10 and 15-17 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Suzuki* (U.S. Patent No. 6,240,524) in view of *Pasqualini* (U.S. Patent Application Publication No. 2002/0023253). Also, claims 11, 14, and 18 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Suzuki* in view of *Pasqualini* and further in view of *Keeth et al.* (U.S. Patent Application Publication No. 2002/0118563). Also, claims 24 and 25 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Keeth et al.* in view of *Pasqualini*. Applicants respectfully traverse these rejections.

### A. Claims 8-14

Independent claim 8 is reproduced below:

8. A method of matching data and clock signal delays within receive logic, comprising the steps of:

minimizing setup and hold times of said receive logic;

***formulating at least one miniaturized version of a clock buffer*** located within said receive logic, wherein ***said at least one miniaturized version of said clock buffer is a scaled down version of said clock buffer***, said miniaturized version of said clock buffer having a scaling factor of K, said scaling factor representing a number of said miniaturized clock buffers utilized to minimize negative variations experienced by said clock buffer; and

minimizing negative variations experienced by said clock buffer.
(Emphasis added)

*Suzuki*, *Pasqualini*, and *Keeth et al.*, taken alone or in combination, fail to teach or suggest the above-highlighted features of independent claim 8. Although *Suzuki* appears to teach clock buffers, it is clear that the clock buffers are scaled to the same size as the other clock buffers. They are not a ***miniaturized version*** or ***scaled down version*** as claimed. *Pasqualini* appears to be silent concerning the scaling of clock buffers and fails to teach or suggest miniaturized or scaled down versions of the clock buffers. In addition, *Keeth et al.* also fails to teach or suggest the claimed feature. *Keeth et al.* instead appears to simply provide a circuit where the conductive paths have the same length, but is silent regarding the above claimed features. Thus, *Keeth et al.* fails to overcome the deficiencies of *Suzuki* and *Pasqualini*.

For at least these reasons, it is believed that the prior art references, when combined, fail to teach or suggest the features of claim 8. Applicants therefore respectfully request that Examiner withdraw the rejection. Also, claims 9-14 are believed to be allowable for at least the reason that they depend directly or indirectly from allowable independent claim 8.

**B. Claims 15-20**

Independent claim 15 is reproduced below:

15. A system for matching data and clock signal delays within receive logic, comprising:

means for minimizing setup and hold times of said receive logic;

***means for formulating at least one miniaturized version of a clock buffer*** located within said receive logic, wherein ***said at least one miniaturized version of said clock buffer is a scaled down version of said clock buffer***, said miniaturized

version of said clock buffer having a scaling factor of K, said scaling factor representing a number of said miniaturized clock buffers utilized to minimize negative variations experienced by said clock buffer; and

means for minimizing negative variations experienced by said clock buffer. (Emphasis added)

*Suzuki*, *Pasqualini*, and *Keeth et al.*, taken alone or in combination, fail to teach or suggest the above-highlighted features of independent claim 15. Although *Suzuki* appears to teach clock buffers, it is clear that the clock buffers are scaled to the same size as the other clock buffers. They is not a ***miniaturized version*** or ***scaled down version*** as claimed. *Pasqualini* appears to be silent concerning the scaling of clock buffers. In addition, *Keeth et al.* also fails to teach or suggest the claimed feature. *Keeth et al.* appears instead to provide a circuit where the conductive paths have the same length, and is silent regarding the above claimed features. Thus, *Keeth et al.* fails to overcome the deficiencies of *Suzuki* and *Pasqualini*.

For at least these reasons, it is believed that the prior art references, when combined, fail to teach or suggest the features of claim 15. Applicants therefore respectfully request that Examiner withdraw the rejection. Also, claims 16-20 are believed to be allowable for at least the reason that they depend directly or indirectly from allowable independent claim 15.

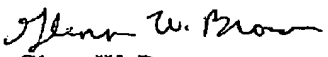
### C. Claims 21-23 and 25-27

As mentioned above with respect to the remarks regarding the 35 U.S.C. §102(e) rejection, it is believed that *Keeth et al.* fails to teach or suggest a system ***wherein each of the at least one data delay device is a scaled down version of the at least one clock buffer with respect to size, power, and load.*** Furthermore, Applicants assert that *Pasqualini* fails to overcome the deficiencies of *Keeth et al.* Particularly, *Pasqualini* appears to be silent concerning a data delay device that is a scaled down version of a clock buffer with respect to size, power, and load. For at least the reason that the combination of references fails to teach or suggest this claimed feature, it is believed that claim 21 is allowable over the prior art of record. Therefore, Applicants respectfully request that the Examiner kindly withdraw the rejection.

## *CONCLUSION*

In light of the foregoing amendments and for at least the reasons set forth above, Applicants respectfully submit that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 8-23 and 25-27 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned at (770) 933-9500.

Respectfully submitted,



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